The following Listing of Claims will replace all prior versions, and listings, of claims in the application.

LISTING OF CLAIMS:

1. (Currently Amended) A data conversion system in which one of a plurality of nodes on an IEEE1394 bus serves as a cycle master, transmits data from one of the plurality of nodes to another node of the plurality of nodes at a transfer rate ~~in synchronism~~ synchronized with a cycle start packet output from the cycle master, and converts the data in the other node of the plurality of nodes, wherein

a first node of the plurality of nodes comprises

an external synchronizing signal receiver for receiving an external reference signal provided on at least one of the first and second nodes, and

a synchronization adjustment unit for controlling the frequency of the cycle start packet output from the cycle master, and linking the frequency of the cycle start packet with the frequency of the reference signal received by the external synchronizing signal receiver, and

said first node or a second node of the plurality of nodes comprises a data conversion unit for converting the data and outputting the converted data at an output rate synchronized ~~in synchronism~~ with the reference signal.

2. (Previously Presented) The data conversion system according to claim 1, wherein

the transmitted data and the converted data are image data, and

the transmitted image data is a video signal in DV format and the converted image data is an analog video signal or SDI video signal.

3. (Previously Presented) The data conversion system according to claim 1, wherein the first node serves as cycle master for data transfer.

4. (Currently Amended) The data conversion system according to claim 1, wherein

the second node comprises ~~the~~ a second synchronization adjustment unit, ~~and~~

the frequency of the cycle start packet ~~frequency~~ is ~~controlled to be~~ linked with the frequency of the reference signal ~~received by the external synchronizing signal receiver~~ by ~~means of~~ the synchronization adjustment unit of the node that serves as the cycle master~~, and is outputted~~.

5 - 7. (Cancelled)

8. (Previously Presented) A device for transmitting a cycle start packet serving as a cycle master on an IEEE1394 bus, receiving data transmitted from a node connected on the IEEE1394 bus at a transfer rate that is ~~in synchronism~~ synchronized with a frequency of the cycle start packet, and converting the received data comprising:

an external synchronizing signal receiver for receiving a reference signal;

a data conversion unit for converting the received data and outputting the converted data at an output rate synchronized with the frequency of ~~in synchronism with~~ the reference signal; and

a synchronization adjustment unit for controlling the frequency of the cycle start packet output from the cycle master ~~linking~~ and linking the frequency of the cycle start packet with the frequency of the reference signal.

9. (Previously Presented) The device according to claim 8, wherein

the received data is image data, and

the received image data is a video signal in DV format, and the data outputted is an analog video signal or SDI signal.

10. (Cancelled)

11. (New) The device according to claim 1, wherein

the second node of the plurality of nodes includes the cycle master and the frequency of the cycle start packet outputted from the cycle master is controlled by the synchronization adjustment unit of the first node.

12. (New) The device according to claim 1, wherein

the synchronization adjustment unit for controlling the frequency of the cycle start packet output from the cycle master is located at a first node and the cycle master is located at a second node in communication with the first node.